Computer System Architecture (BHCS02) Discipline Specific Core Course - (DSC) Credit: 06

Course Objective

This course introduces the students to the fundamental concepts of digital computer organization, design and architecture. It aims to develop a basic understanding of the building blocks of the computer system and highlights how these blocks are organized together to architect a digital computer system.

Course Learning Outcomes

On successful completion of the course, students will be able to:

1. Design Combinational Circuits using basic building blocks. Simplify these circuits using Boolean algebra and Karnaugh maps. Differentiate between combinational circuits and sequential circuits.
2. Represent data in binary form, convert numeric data between different number systems and perform arithmetic operations in binary.
3. Determine various stages of instruction cycle and describe interrupts and their handling.
4. Explain how CPU communicates with memory and I/O devices.
5. Simulate the design of a basic computer using a software tool

Detailed Syllabus

Unit 1

Digital Logic Circuits: Logic Gates, truth tables, Boolean Algebra, digital circuits, combinational circuits, sequential circuits, circuit simplification using Karnaugh map, Don't Care Conditions, flip-flops, characteristic tables

Unit 2

Digital Components: Half Adder, Full Adder, Decoders, Multiplexers, Registers and Memory Units

Unit 3

Data Representation and Basic Computer Arithmetic: Number system, complements, fixed and floating point representation. Alphanumeric representation. Addition, subtraction.

Unit 4

Basic Computer Organization and Design: Common Bus system, instruction codes, instruction format, instruction set completeness, Sequence Counter, timing and control, instruction cycle, memory reference instructions and their implementation using arithmetic, logical, program control, transfer and input output micro-operations, interrupt cycle.

Unit 5

Central Processing Unit: Micro programmed Control vs Hardwired Control, lower level programming languages, Instruction format, accumulator, general register organization, stack organization, zero-address instructions, one-address instructions, two-address instructions, three-address instructions, Addressing Modes, RISC, CISC architectures, pipelining and parallel processing.

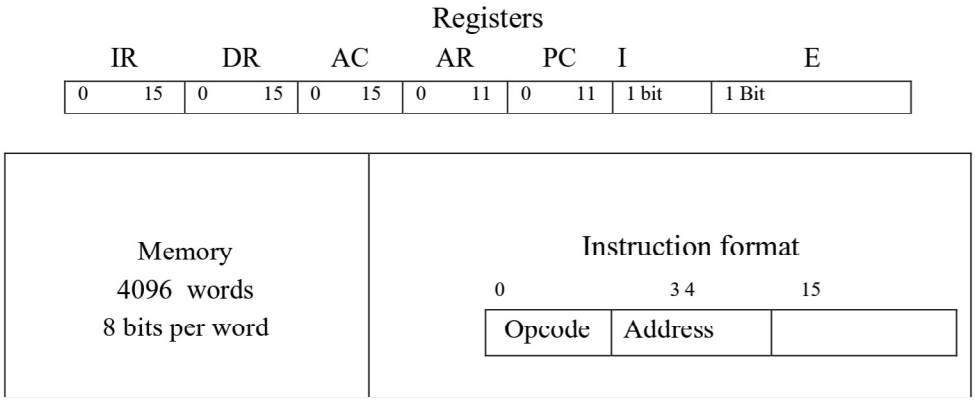
Unit 6

Memory Organization and Input-Output Organization: Input-Output Organization: Peripheral Devices, I/O interface, I/O vs. Memory Bus, Programmed I/O, Interrupt-Driven I/O, Direct Memory Access

Practical

(Use Simulator – CPU Sim 3.6.9 or any higher version for the implementation)

1. Create a machine based on the following architecture :



Basic Computer Instructions

Memory Reference			Register Reference		
Symbol	Hex		Symbol	Hex	
AND	0xxx	Direct Addressing	CLA	E800	
ADD	2xxx		CLE	E400	
LDA	4xxx		CMA	E200	
STA	6xxx		CME	E100	
BUN	8xxx		CIR	E080	
			CIL	E040	
ISZ	Cxxx		INC	E020	
AND_I	1xxx	Indirect Addressing	SPA	E010	
ADD_I	3xxx		SNA	E008	
LDA_I	5xxx		SZA	E004	
STA_I	7xxx		SZE	E002	
BUN_I	9xxx		HLT	E001	
ISZ_I	Dxxx				

Refer to Chapter-5 of reference 1 for description of instructions.

Design the register set, memory and the instruction set. Use this machine for the assignments of this section.

2. Create a Fetch routine of the instruction cycle.
3. Write an assembly program to simulate ADD operation on two user-entered numbers.
4. Write an assembly program to simulate SUBTRACT operation on two user-entered numbers.
5. Write an assembly program to simulate the following logical operations on two user-entered numbers.
    1. AND
    2. OR
    3. NOT
    4. XOR
    5. NOR
    6. NAND
6. Write an assembly program to simulate MULTIPLY operation on two user-entered numbers.
7. Write an assembly program for simulating following memory-reference instructions.
    1. ADD
    2. LDA
    3. STA
    4. BUN
    5. ISZ
8. Write an assembly language program to simulate the machine for following register reference instructions and determine the contents of AC, E, PC, AR and IR registers in decimal after the execution:

1. CLA
2. CMA
3. CME
4. HLT

9. Write an assembly language program to simulate the machine for following register reference instructions and determine the contents of AC, E, PC, AR and IR registers in decimal after the execution:

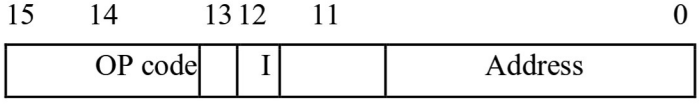
1. INC
2. SPA
3. SNA
4. SZE

10. Write an assembly language program to simulate the machine for following register reference instructions and determine the contents of AC, E, PC, AR and IR registers in decimal after the execution:

1. CIR
2. CIL

11. Write an assembly program that reads in integers and adds them together; until a negative non-zero number is read in. Then it outputs the sum (not including the last number).
12. Write an assembly program that reads in integers and adds them together; until zero is read in. Then it outputs the sum.
13. Create a machine for the following instruction format:

Instruction format



The instruction format contains a 3-bit opcode, a 1-bit addressing mode and a 12-bit address.

Write an assembly program to simulate the machine for addition of two numbers with I= 0 (Direct Address) and address part = 082. The instruction to be stored at address 022 in RAM, initialize the memory word with any decimal value at address 082. Determine the contents of AC, DR, PC, AR and IR in decimal after the execution.

14. Simulate the machine for the memory-reference instruction referred in above question with I= 1 (Indirect Address) and address part = 082. The instruction to be stored at address 026 in RAM. Initialize the memory word at address 082 with the value 298. Initialize the memory word at address 298 with operand 632 and AC with 937. Determine the contents of AC, DR, PC, AR and IR in decimal after the execution.

15. The instruction format contains 3 bits of opcode, 12 bits for address and 1 bit for addressing mode. There are only two addressing modes, I = 0 is direct addressing and I = 1 is indirect addressing. Write an assembly program to check the I bit to determine the addressing mode and then jump accordingly.

References

1. Mano, M. (1992). *Computer System Architecture*. 3rd edition. Pearson Education.

Additional Resources

1. Mano, M. (1995). *Digital Design*. Pearson Education Asia.
2. Null, L., & Lobur, J. (2018). *The Essentials of Computer Organization and Architecture*. 5th edition. (Reprint) Jones and Bartlett Learning.
3. Stallings, W. (2010). *Computer Organization and Architecture Designing for Performance* 8th edition. Prentice Hall of India.

Course Teaching Learning Process

- Use of ICT tools in conjunction with traditional class room teaching methods
- Interactive sessions
- Class discussions

Tentative weekly teaching plan is as follows:

Week	Content
1 – 2	Unit 1 - Introduction: Digital Logic Gates, Flipflops and their characterstic table, Logic circuit simplification using Boolean Algebra and Karnaugh Map, Don't Care conditions. Combinational Circuits, Sequential Circuits.
3 – 4	Unit 2 - Digital Components: Decoders, Encoders, Multiplexers, Binary Adder, Binary Adder-Subtractor, Binary Incrementer, Registers and Memory Units
5 – 6	Unit 3 - Data Representation:

	Binary representation of data, representation of alpha data, representation of numeric data in different number systems, conversion between number systems, complements, representation of decimal numbers, representation of signed and unsigned numbers, addition and subtraction of signed and unsigned numbers and overflow detection.
7 – 11	Unit 4 - Operations and Control: Arithmetic and logical micro-operations, micro programmed control vs. hardwired control, instruction format, instruction set completeness, timing and control, instruction cycle, memory reference instructions and their implementation using arithmetic, logical, program control, transfer and input output micro operations, interrupt cycle.
12 - 13	Unit 5 - Instructions: Instruction format illustration using single accumulator organization, general register organization and stack organization, Addressing Modes, zero-address instructions, one-address instructions, two-address instructions and three-address instructions,
14 - 15	Unit 6 - Peripheral Devices: I/O interface, I/O vs. Memory Bus, Isolated I/O, Memory Mapped I/O, Direct Memory Access

Assessment Methods

Written tests, assignments, quizzes, presentations as announced by the instructor in the class.

Keywords

Combinational and sequential circuits, memory organization, computer organization, CPU design, parallelism.

Programming in JAVA (BHCS03) Discipline Specific Core Course - (DSC)

Credit: 06
